

CLAIMS

1. A method of simultaneously synchronizing multiple input signals to multiple output signals, comprising:
 - communicating a plurality of signal pairs each comprising a clock input
 - 5 and a signal input;
 - providing a discrete-time phase detector, loop filter, and voltage controlled oscillator that together operate as a single discrete-time phase locked loop in hardware for calculating an output signal from an input signal;
 - providing a control logic;
 - 10 providing a context memory (RAM) for storing a history for each of the respective signal pairs;
 - and, upon receipt at the discrete-time phase detector of the clock signal of a respective one of the signal pairs, operating the control logic:
 - to retrieve from the context memory the history for the
 - 15 respective signal pair,
 - to enable the discrete-time phase locked loop to calculate from the respective input signal a respective output signal thus defining a resulting history for the respective input signal,
 - and to store the resulting history in the context memory for use
 - 20 in subsequent calculations for the respective input signal pair.
2. The method according to Claim 1 wherein the Context memory is arranged to store and retrieve a history from the loop filter and a history from the Voltage Controlled Oscillator of the discrete-time phase locked loop.

3. The method according to Claim 1 wherein there is provided a high speed clock signal which is supplied to the control logic to control routing of input signals to the discrete-time Phase Locked Loop, retrieving of the history from the Context memory RAM, writing of the history into the loop filter and Voltage
- 5 Controlled Oscillator registers of the discrete-time PLL, triggering of the discrete-time Phase Locked Loop stages, storing of the history from the loop filter and Voltage Controlled Oscillator registers into the Context RAM, and routing of the output signal to a respective output port.